



Figure 1

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graph TD
    A[Receive line of information from a processor 210] --> B[Store line of information in a cache 220]
    B --> C{Line of information disposable? 230}
    C -- No --> D[Write line of information to system memory 240]
    C -- Yes --> E{Line of information read by a system device? 250}
    E -- No --> C
    E -- Yes --> F[Overwrite cache entry containing line of information without first writing line of information to system memory 260]

```

Figure 2